WHAT IS CLAIMED IS:

1. A method for distributed device identifier number assignment and device counting in a serially connected chain of devices, comprising:

receiving a first sequence of received pulses;

determining a unique device identifier based upon the first sequence received of pulses;

transmitting a first sequence of transmitted pulses;

receiving a second sequence of received pulses;

transmitting a second sequence of transmitted pulses; and

determining a total device count based upon the first and second sequences of received pulses.

2. The method of claim 1, further comprising the step of initializing a first and a second memory locations before receiving the first sequence of received pulses.

3. The method of claim 2, wherein the first and second memory locations are both initialized to a value that is equal to a maximum allowed number of devices in the serially connected chain.

4. The method of claim 3, wherein the determining a unique device identifier step comprises:

counting a number of pulses in the first sequence of received pulses; and

subtracting the number of pulses from the value stored in the first memory location.

5. The method of claim 4, wherein the unique device identifier is stored back to the first memory location.

6. The method of claim 3, wherein the determining a total device count comprises:

counting the number of pulses in the second sequence of received pulses;

subtracting the number of pulses from the value stored in the second memory location to obtain a difference; and

adding the value stored in the first memory location and the difference.

7. The method of claim 6, further comprising incrementing the result of adding the value stored in the first memory location and the difference by one (1.0).

8. The method of claim 1, wherein the first sequence of transmitted pulses is a sequence of pulses with one pulse less than the number of pulses in the first sequence of received pulses.

9. The method of claim 1, wherein the second sequence of transmitted pulses is a sequence of pulses with one pulse less than the number of pulses in the second sequence of received pulses.

10. The method of claim 1, wherein the receiving first received sequence and the transmitting first transmitted sequence are received and transmitted over different input/output connections.

11. The method of claim 1, wherein the receiving second received sequence and the transmitting second transmitted sequence are received and transmitted over different input/output connections.

12. The method of claim 1, wherein the receiving first received sequence and transmitting second transmitted sequence are received and transmitted over the same input/output connection.

13. The method of claim 1, wherein the transmitting first transmitted sequence and receiving second received sequence are received and transmitted over the same input/output connection.

14. A semiconductor device comprising:

a counter, coupled to an input/output node, the counter for counting a number of pulses in a sequence of pulses received at the input/output node;

a first storage location to store a first count result; and

a pulse generator, for generating a specified length sequence of pulses, the specified length being one less than the number of pulses in the sequence of pulses received at the input/output node.

15. The semiconductor device of claim 14, wherein the semiconductor device uses the first count result as a device identifier.

16. The semiconductor device of claim 14, wherein a second sequence of pulses is received at a second input/output node.

17. The semiconductor device of claim 16, further comprising a second storage location to store a second count result.

18. The semiconductor device of claim 17, wherein the first and second count results are combined to provide information on a total number of devices in a system that includes the semiconductor device.

19. The semiconductor device of claim 14, further comprising a controller, coupled to the first storage location, the counter and the pulse generator, the controller controlling the operation of the counter and the pulse generator.

20. The semiconductor device of claim 19, wherein the controller is a microcontroller.

21. The semiconductor device of claim 19, wherein the controller is a microprocessor.

22. The semiconductor device of claim 19, wherein the controller is a finite state machine.

23. A system comprising:

a processor, coupled to a sequence of least one codec, adapted to processing digital data;

a controller, coupled to the sequence of at least one codec, adapted to controlling communications between the processor and the sequence of at least one codec;

the sequence of at least one codec, each codec comprising:

a port coupled to the processor and the controller; and

a semiconductor device for distributed device identifier number assignment and device counting coupled to the port.

24. The system of claim 23, wherein the semiconductor device further comprising:

a counter, coupled to an input/output node, the counter for counting a number of pulses in a sequence of pulses received at the input/output node;

a first storage location to store a first count result; and

a pulse generator, for generating a specified length sequence of pulses, the specified length being one less than the number of pulses in the sequence of pulses received at the input/output node.

25. The system of claim 23, wherein a FSD signal line of a final codec in the sequence of at least one codec is connected to an external pulse generator.

26. The system of claim 23, wherein the semiconductor device operates each time the system is reset.

27. The system of claim 23, wherein the semiconductor device operates each time the system is powered-up.

28. A method for providing a variable number of time slots within a synchronization period in a system with at least one communicating device, the method comprising:

determining a number of desired time slots;

programming a programmable data clock driving the transmission of data to a multiple of a timing clock driving the synchronization period; and

configuring a delay for each semiconductor device proportional to a number of time slots assigned to each communicating device.

29. The method of claim 28, wherein the multiple is equal to the number of desired time slots multiplied by a number of bits per time slot.

30. The method of claim 28, wherein the delay for each communicating device may be different for each communicating device.

31. The method of claim 28, further comprising the step of assigning the delay for each communicating device to each communicating device.

32. The method of claim 28, wherein the programming a programmable data clock step comprises:

calculating a frequency for the programmable data clock; and

setting the programmable data clock to operate at the calculated frequency.

33. The method of claim 32, wherein the calculated frequency is equal to the timing clock frequency multiplied by the number of communicating devices in system multiplied by the number of time slots per communicating device multiplied by the number of bits per time slot.

34. The method of claim 32, wherein the programmable data clock is set to operate at a second frequency, wherein the second frequency is greater than the calculated frequency.

35. A semiconductor device comprising:

a programmable data clock, including an output that provides a clock to time the transmission of data;

a calculator unit, for calculating an operating frequency of the programmable data clock based on a desired number of time slots; and

a delay insertion unit, coupled to the calculator unit and a sequence of at least one communicating device, the delay insertion unit providing each communicating device a delay proportional to a number of time slots assigned to each communicating device.

36. The semiconductor device of claim 35, wherein the calculator unit is a microcontroller.

37. The semiconductor device of claim 35, wherein the calculator unit is a microprocessor.

38. The semiconductor device of claim 35, wherein the semiconductor device is internal to a processor.

39. The semiconductor device of claim 35, wherein the semiconductor device is external to a processor.

40. The semiconductor device of claim 35, wherein the communicating device is a coder/decoder (codec).

41. A system comprising:

a sequence of at least one communicating device;

a processor, coupled to the sequence of at least one communicating device, adapted to processing digital data, the processor further comprising;

a programmable data clock, including an output that provides a clock to time the transmission of data;

a calculator unit, for calculating an operating frequency of the programmable data clock based on a desired number of time slots; and

a delay insertion unit, coupled to the calculator unit and a sequence of at least one communicating device, the delay insertion unit providing each communicating device a delay proportional to a number of time slots assigned to each communicating device.

42. The system of claim 41, wherein the delay assigned to each communicating device may be different based on a number of time slots assigned to each communicating device.

43. The system of claim 41, wherein the sequence of at least one communicating device is a sequence of serially connected communicating devices.

44. The system of claim 41, wherein the programmable data clock is set to operate at a frequency that is greater than the operating frequency calculated by the calculator unit.

45. The system of claim 41, wherein the communicating device is a coder/decoder (codec).

46. The system of claim 41, wherein communications between the processor and the sequence of at least one communicating device is performed using a time division multiplexed connection.

47. The system of claim 46, wherein the time division multiplexed connection is a serial connection.